BH9914A
GPIB embedded module

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FEATURES:
• controller or talker/listener
• TMS9914 Texas Instruments or NAT9914 National Instruments populated
• 8 bits data bus
• 3 bits GPIB address
• DMA transfer possible
• optionally GPIB signals header
• local oscillator in range 1 MHz – 20 MHz
• local or remote RESET
• TTL compatible Inputs/Outputs
• +5V operation (V_{DD}-V_{SS})

DESCRIPTION:
The BH9914A is an embedded GPIB module (also known IEEE488.2 or HP-IB). It can be ordered as controller or talker/listener only and populated either with socket only or TMS9914A (Texas Instruments) or NAT9914A (National Instruments). The clock and reset signal can be generated either locally or used from MCU/CPU system.

I/O CONNECTOR SIGNALS:
I/O connector (J2) signals are on CPU / MCU side available on 26-pin flat cable connector or header.

V_{DD} (Pin 1, Pin 2)
Positive Supply Voltage. From +4.5V to +5.5V.

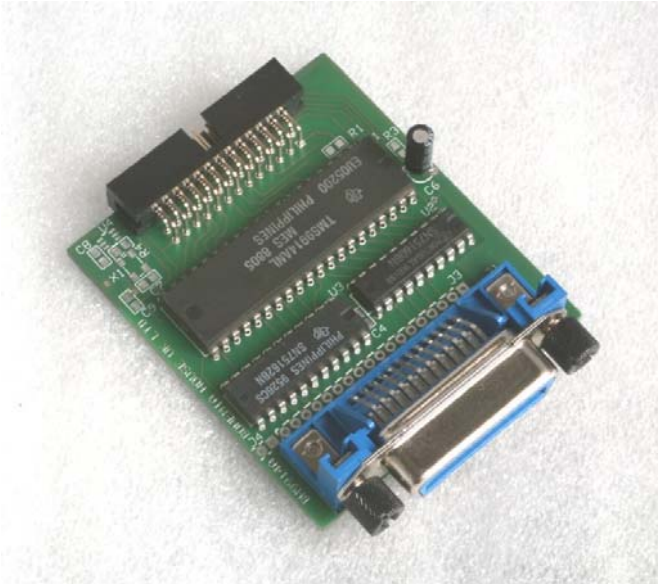
$\overline{ACCGR}$ (Pin 3) - Input
Access Granted: when received from the DMA control logic this enables the byte onto the data bus. $\overline{ACCGR}$ must be high when not participating in DMA transfer.

$\overline{ACCRQ}$ (Pin 4) - Output
Access Request: signal becomes active (low) to request a DMA

SC (Pin 5) - Input
System Controller: this signal is available only if the module is populated as controller. Default must be high. If switched to low, the module works as non-system controller only.

NC (Pin 6) – not connected

$\overline{RESET}$ (Pin 7) - Input/Output
Reset: this pin is input if the reset logic is not populated, otherwise is output. Active low. Initializes the module at power-on.



ORDER CODE:

BH9914AC-M-RC-X-H	controller
BH9914AT-M-RC-X-H	talker/listener

M is **mfg of GPIB controller**:

T	Texas Instruments
N	National Instruments
S	socket only

RC is **oscillator frequency** in range 1 to 20 MHz, ie:

00	no oscillator
02	2 MHz (or a number in range from 01 to 20)

X is **I/O connector** option:

0	angle male flat cable connector, top side
1	straight male flat cable connector, top side
2	angle male flat cable connector, bottom side
3	straight male flat cable connector, bottom side
4	angle header, top side
5	straight header, top side
6	angle header, bottom side
7	straight header, bottom side

H is **GPIB option header** (on bottom side only):

0	GPIB header not populated
1	GPIB header populated

NC (Pin 8) – not connected

NC (Pin 9) – not connected

GND (Pin 10)
Ground reference voltage.

READ/$\overline{\text{WRITE}}$ (Pin 11) - Input
Read / Write: when active (low), indicates to the module that data is being written to one of its registers.

$\overline{\text{CE}}$ (Pin 12) - Input
Chip Enable: when active (low), allows access to the module read and write registers. If this signal is high, the D0-D7 pins are in high impedance unless $\overline{\text{ACCGR}}$ is low.

RS0 (Pin 13) - Input
Register Select Line: LSB, determine which register is addressed by MPU / CPU during a read or write operation.

DBIN (Pin 14) - Input
Data Bus In: an active (high) state indicates to the module that a read is about to be carried out by MPU / CPU.

RS2 (Pin 15) - Input
Register Select Line: MSB

RS1 (Pin 16) - Input
Register Select Line: middle bit

D0 (Pin 17) - Input/Output
Data 0: data transfer line on MPU / CPU side

$\overline{\text{INT}}$ (Pin 18) - Output
Interrupt: sent to the MPU / CPU to cause a branch to service routine

D2 (Pin 19) - Input/Output
Data 2: data transfer line on the MPU / CPU side

D1 (Pin 20) - Input/Output
Data 1: data transfer line on the MPU / CPU side

D4 (Pin 21) - Input/Output
Data 4: data transfer line on the MPU / CPU side

D3 (Pin 22) - Input/Output
Data 3: data transfer line on the MPU / CPU side

D6 (Pin 23) - Input/Output
Data 6: data transfer line on the MPU / CPU side

D5 (Pin 24) - Input/Output
Data 5: data transfer line on the MPU / CPU side

CLK (Pin 25) - Input/Output
Clock: this pin is input if a local oscillator is not populated, otherwise is output. Clock signal, 500 kHz minimum, Not need be synchronous to system clock.

D7 (Pin 26) - Input/Output
Data 7: data transfer line on the MPU / CPU side

GPIB HEADER SIGNALS:
GPIB header (J3) signals can be used for GPIB bus monitoring. If this header is installed, it is accessible on bottom side only.

V_{DD} (Pin 1)
Positive Supply Voltage. From +4.5V to +5.5V.

DIO5 (Pin 2)
Data Input Output 5: data line on the GPIB bus

DIO6 (Pin 3)
Data Input Output 6: data line on the GPIB bus

DIO7 (Pin 4)
Data Input Output 7: data line on the GPIB bus

DIO8 (Pin 5)
Data Input Output 8: data line on the GPIB bus

DIO1 (Pin 6)
Data Input Output 1: data line on the GPIB bus

DIO2 (Pin 7)
Data Input Output 2: data line on the GPIB bus

DIO3 (Pin 8)
Data Input Output 3: data line on the GPIB bus

DIO4 (Pin 9)
Data Input Output 4: data line on the GPIB bus

IFC (Pin 10)
Interface Clear: sent by the system controller to set the interface system into a known quiescent state. The system controller becomes controller in charge.

NDAC (Pin 11)
Not Data Accepted: handshake line. Acceptor sets this false (high) when it has latched the data from I/O lines

ATN (Pin 12)
Attention: sent by controller in charge.. When true (low) interface commands are being sent over the DIO lines. When false (high), these lines carry data.

SQR (Pin 13)
Service Request: set true (low) by a device to indicate to need a service.

NRFD (Pin 14)
Not Ready For Data: handshake line. Sent by acceptor to indicate readiness for the next byte.

DAV (Pin 15)
Data Valid: handshake line controlled by source to show acceptors when valid data are present to the bus.

EOI (Pin 16)
End Of Identify: if ATN is false (high), this indicates end of message block. If ATN is true (low), the controller is requesting a parallel poll.

REN (Pin 17)
Remote Enable: sent by system controller to select control either from the front panel or from the IEEE bus.

GND (Pin 18)
Ground reference voltage.

J4 JUMPER:
If J4 is on, the shield of GPIB cable is connected to ground.

ABSOLUTE MAXIMUM RATINGS:

Ambient temperature ..... 0°C to +70°C
Storage temperature ..... -55°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +5.5V
Voltage on inputs with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation ..... 1.2 Watt
Maximum current out of V_{SS} pin, 0°C ≤ T_A ≤ +70°C ..... 200 mA

RECOMMENDED OPERATING CONDITIONS:
(All voltages referenced to V_{SS}, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	V_{DD}	4.5	5.5	V	
Supply Voltage	V_{SS}		0	V	
Logic Low	V_{IL}	V_{SS} -0.3	0.8	V	
Logic High	V_{IH}	2	5.5	V	

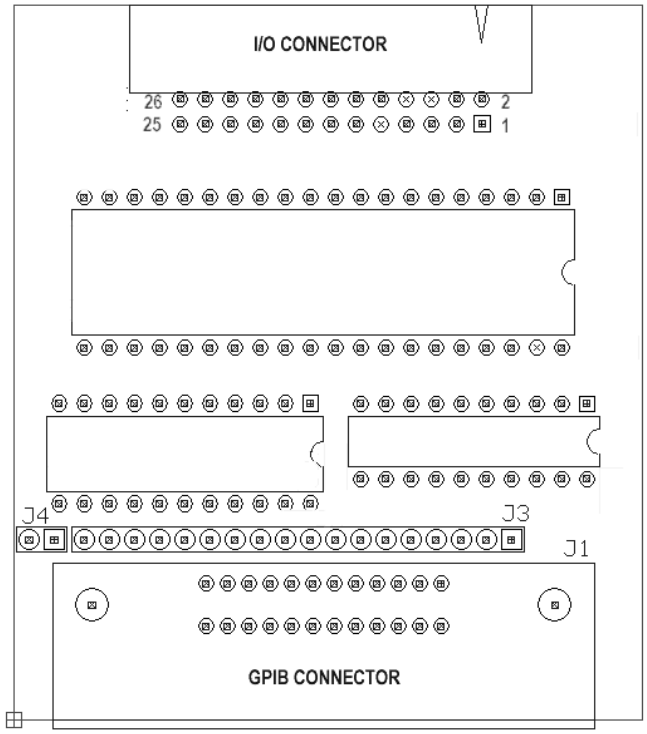


Figure 1 – BH9914A top layout, component view

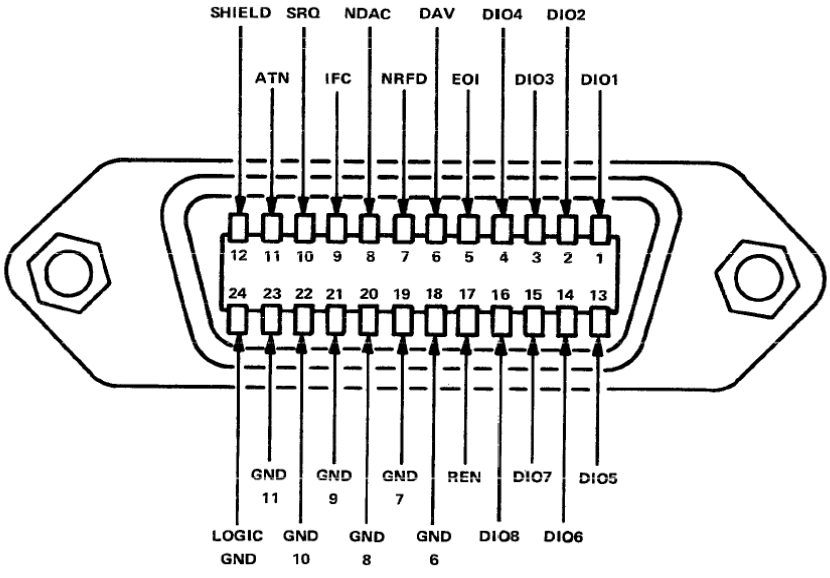


Figure 2 – GPIB connector